**REMARKS**

Claims 1-33 are pending, of which claims 1, 7, 12, 20, 26, and 31 are in independent form.

Claims 1, 2, 7, 9, 12, 13, 20, 26, 27, 28, 31, and 33 have been amended by way of the present response.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

**Regarding the Specification**

Responsive to the comments in the pending Office Action regarding the disclosure, Applicant has appropriately amended Paragraphs [0001] and [0034] of the specification. It is therefore believed that the pending objections to the disclosure have been overcome.

**Regarding the Claim Objections**

Claims 12-19 and 26-30 have been objected to because of certain informalities. Applicant has appropriately amended the claims in response to the comments provided in the pending Office Action in this regard. It is therefore believed that the pending claim objections have been overcome by the present response.

**Regarding the Claim Rejections**

In the pending Office Action, claims 1-33 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,815,402 to Taylor et al. (the *Taylor* reference). In connection with these §102(b) rejections, the Examiner has commented as follows:

> As per **claims 1,7-9,12,20-21,25-26,31-33**, all of the elements of the claims are illustrated in Figs. 7 and 9, wherein the flat netlist driver (710) reads or traverse the logical representation of the hierarchical design (i.e., schematic netlist) (see steps 904-920 of Fig. 9), which includes reading/loading determining the RC information as parameters (see col. 10, lines 31-42; col. 8, lines 13-47), wherein the flat netlist formatter writes the flat representation of each instantiation to the flat netlist file (col. 10, line 43 to col. 11, line 49), for use by other tools (i.e., other software and tools used by other designers -- col. 1, lines 49-68; Fig. 8, showing at least simulator software, schematic design tool to which the flat netlist is accessible), wherein such flat netlist files can be considered as external since it is at least external to the flat netlist driver and is accessible by other tools or processes; wherein the computer readable medium operable with a computer, containing computer-executable instructions for implementing the method, the system, and the means associated with the system are part of the CAD system (see col. 6, lines 30-47; Fig. 6), being necessary to implement the computer-implemented method.

Applicant respectfully submits that the pending §102(b) rejections have been overcome or otherwise rendered moot by way of the present response. As currently constituted, base claim 1 is directed to an embodiment for enabling a first circuit analysis

tool to flatten a hierarchical design for processing by a second circuit analysis tool, the embodiment including, *inter alia*, identifying a particular block of the hierarchical design to be flattened, wherein the particular block is operable to include any instantiations of child blocks at a level lower than the particular block's level. Additionally, the embodiment of claim 1 includes writing a flat representation of the particular block to a file, wherein the instantiations of the child blocks may be rotated with respect to one another. Substantially similar features are also recited in the remaining base claims, i.e., claims 7, 12, 20, 26, and 31.

The *Taylor* reference provides a system and method for changing the connected behavior of a circuit design schematic (e.g., open or closed switches) by interpreting instance parameters at the time a netlist is being created. See column 2, lines 35-38. Although a flat netlisting traversal driver 710 is provided to determine primitive devices for each instance in a circuit schematic (e.g., schematic 112 in FIG. 3 or FIG. 4) (see column 9, lines 34-48; see also FIG. 7 and FIG. 9), there is no teaching or suggestion in *Taylor* with respect to the claimed features of identifying a particular block of the hierarchical design to be flattened, wherein the particular block is operable to include any

instantiations of child blocks at a level lower than the particular block's level, as well as writing a flat representation of the particular block to a file, wherein the instantiations of the child blocks may be rotated with respect to one another.

At least for the foregoing reasons, base claims 1, 7, 12, 20, 26, and 31, as currently constituted, are believed to be allowable over the applied art of record. Dependent claims 2-6 (depending from base claim 1), dependent claims 8-11 (depending from base claim 7), dependent claims 13-19 (depending from base claim 12), dependent claims 21-25 (depending from base claim 20), dependent claims 27-30 (depending from base claim 26), and dependent claims 32-33 (depending from base claim 31) are also in condition for allowance accordingly.

PATENT APPLICATION
DOCKET NO.: 200311777-1

**SUMMARY AND CONCLUSION**

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

Dated: 6/27/2006

Shreen K. Danamraj
Registration No. 41,696

Correspondence Address

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Please direct telephone calls to:

Leslie Paul Gehman
(970) 898-3642